

FIG. 1 PRIOR ART

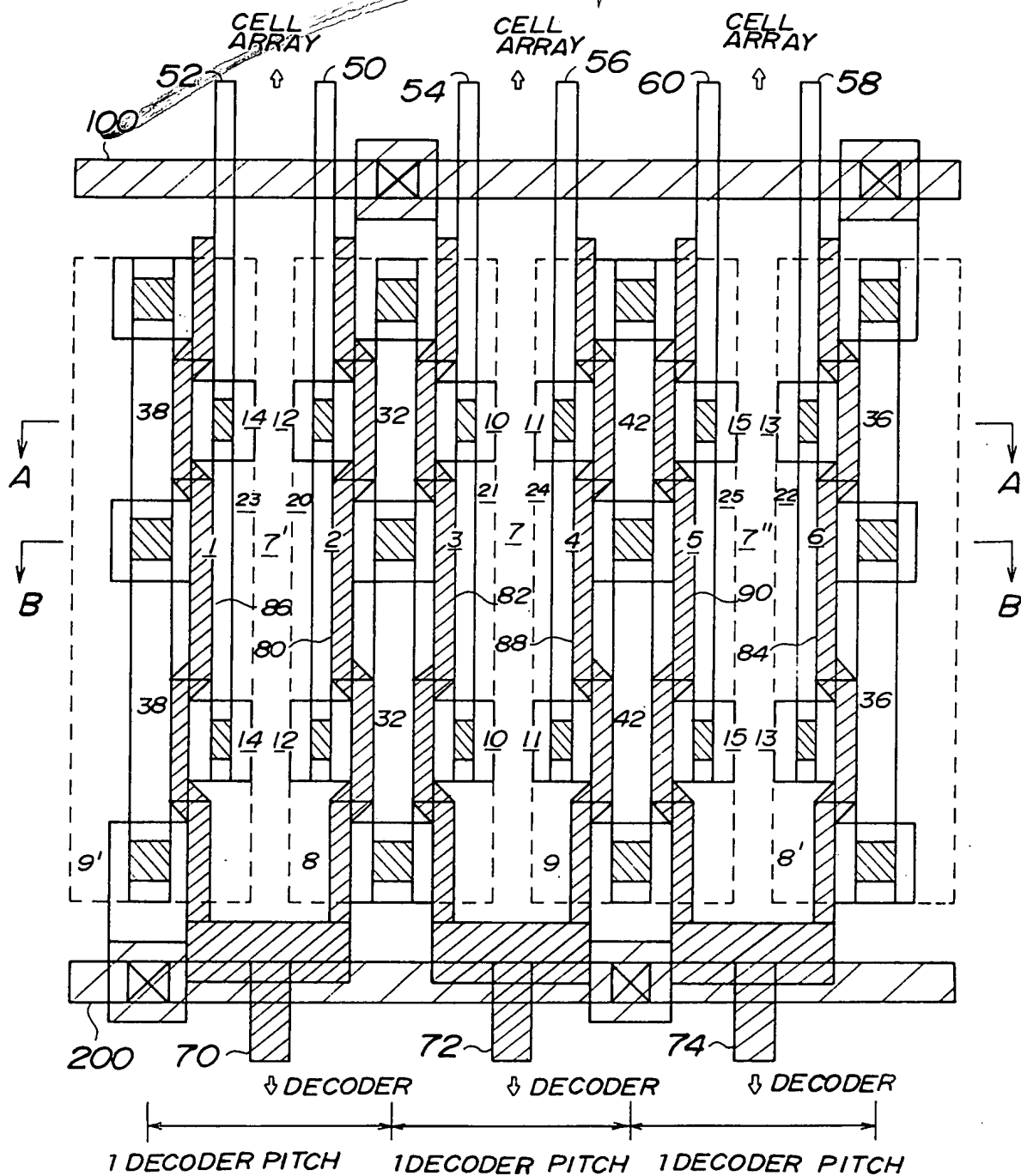


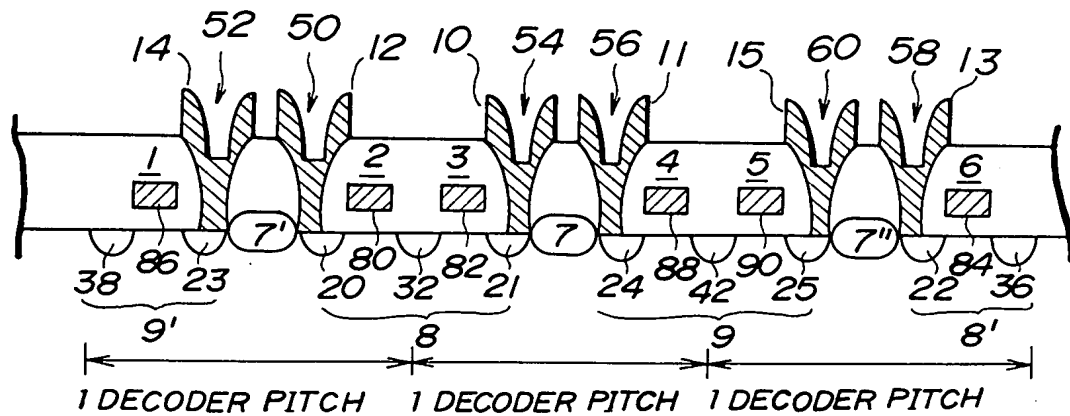
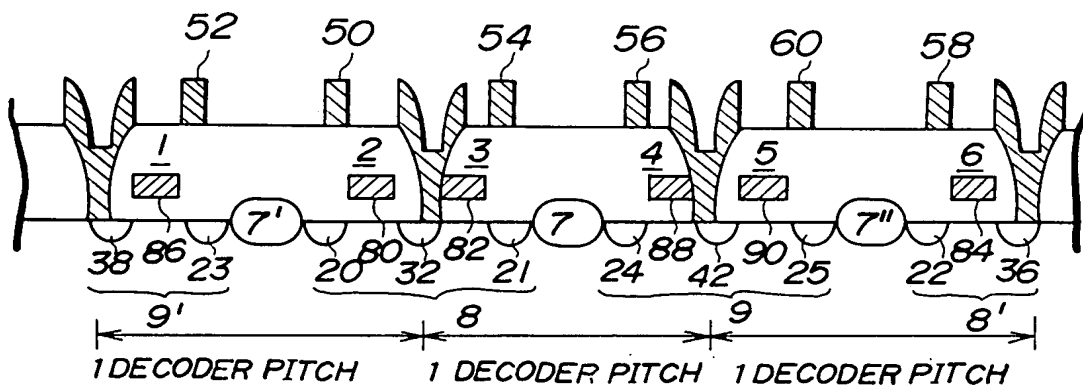
FIG. 2 PRIOR ART**FIG. 3 PRIOR ART**

FIG. 4

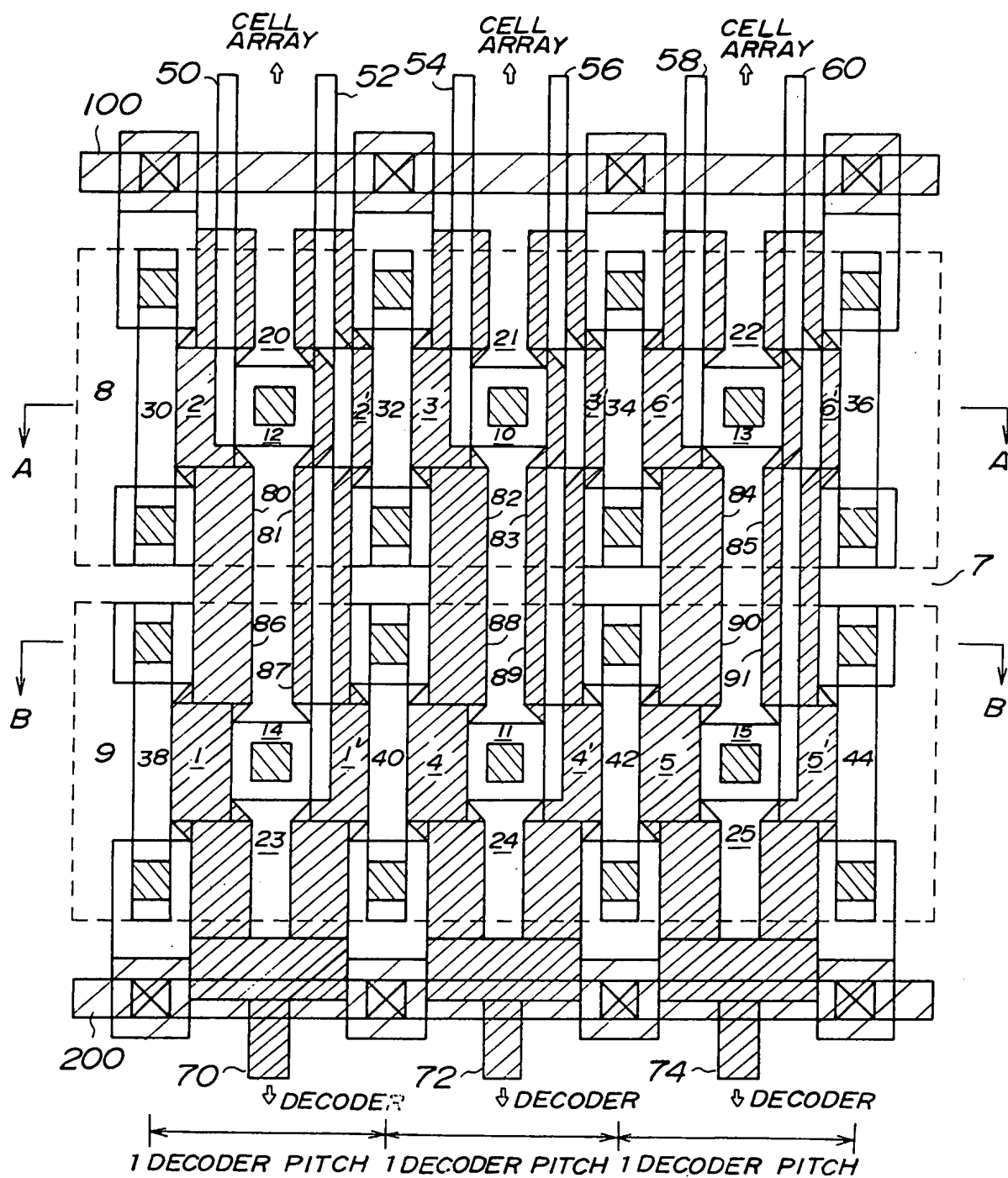


FIG. 5

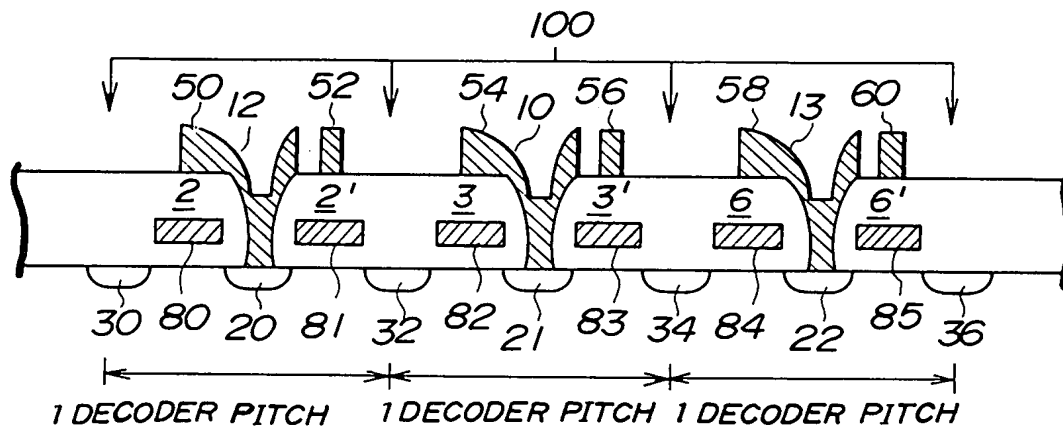
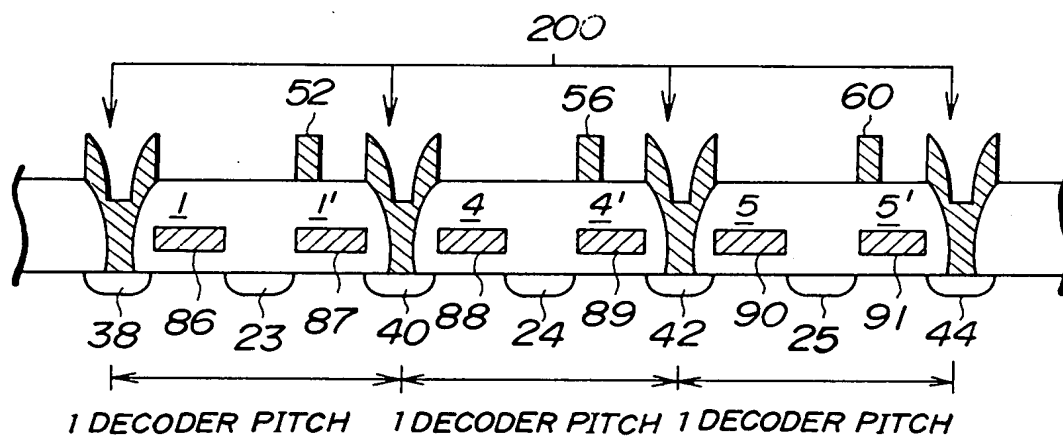


FIG. 6



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FIG. 8

The diagram shows a memory array circuit. On the left, a dashed box labeled '304' contains a 'DECODER' section with inputs $/R$, $A0$, and $A1$. The decoder uses PMOS transistors 300 and 303 and NMOS transistors 301 and 302 to generate signals 307 and 308 . A 'LEVEL SHIFT' section follows, containing PMOS transistors 402 and 403 and NMOS transistors 400 and 401 , along with a capacitor 310 . The output of the level shift is signal 400 . This signal is connected to the gates of PMOS transistors $Q3$ and $Q4$ in the memory array. The array also includes NMOS transistors 305 and 306 , and memory cells connected to a 'BIT LINE' and signals 54 and 56 . The circuit is powered by V_{cc} and V_{ss} .

FIG. 9

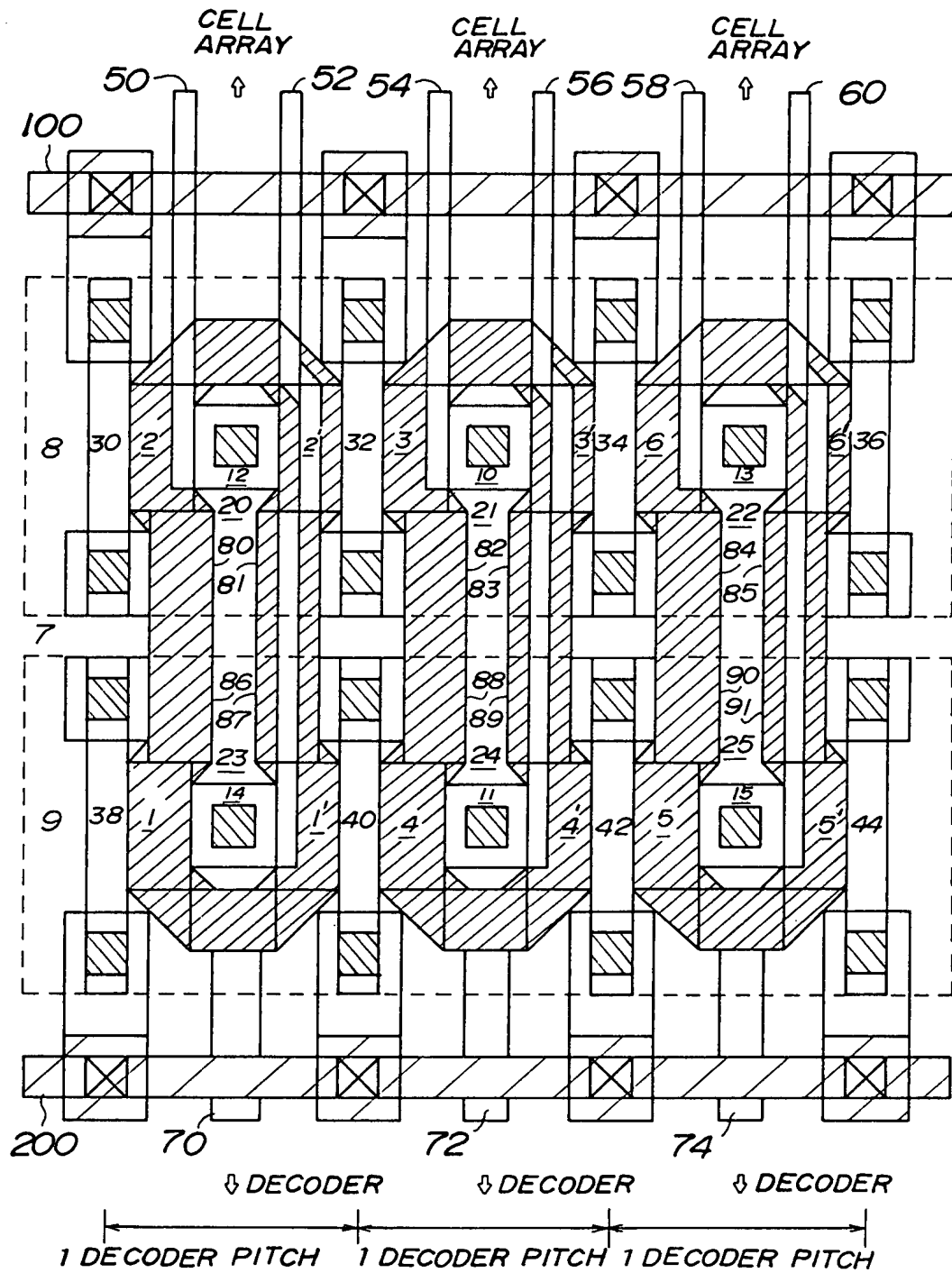


FIG.10

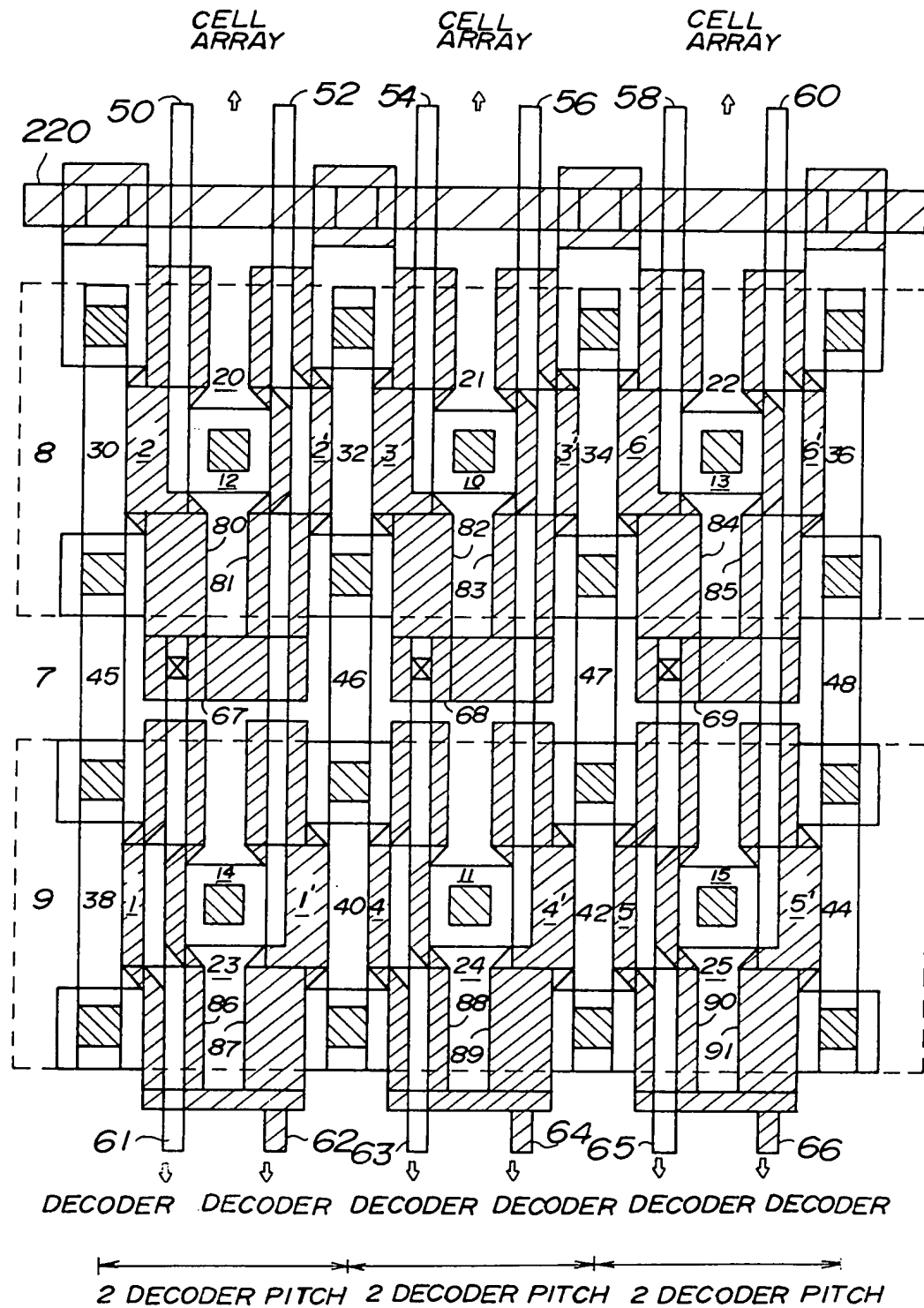


FIG. 11

